

ABSTRACT

A system and method for providing efficient block transfer operations through a test access port uses a Fastdata register. The Fastdata register, in part, emulates a pending process access bit ("PrAcc") typically found in a Control register associated with the test access port. When a Fastdata access (either a Fastdata upload or a Fastdata download) is requested by a probe coupled to the test access port, the Fastdata register is serially coupled to a data register also associated with the test access port. With these registers so coupled and through the operation of the Fastdata register, downloading and uploading data can be accomplished using a single register operation.